IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

COMPUTER CIRCUIT OPERATIONS LLC, Plaintiff, v. NXP USA, INC., NXP SEMICONDUCTORS N.V., AND NXP B.V., Defendants.	Case No.: 6:21-cv-00138 **Jury Trial Demanded**

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Computer Circuit Operations LLC ("CCO") hereby files Complaint for patent infringement against Defendants NXP USA, Inc., NXP Semiconductors N.V., and NXP B.V. (collectively, "NXP" or "Defendants") and alleges as follows:

PARTIES

1. Plaintiff CCO is a limited liability company organized and existing under the laws of the State of New York, having its principal place of business at 1629 Sheepshead Bay Road, Floor 2, Brooklyn, New York, 11235.

2. On information and belief, NXP USA, Inc. is a Delaware corporation having its principal place of business at 6501 William Cannon Drive West, Austin, TX 78735. NXP USA, Inc. may be served with process through its registered agent Corporation Service Company d/b/a CSC - Lawyers Incorporating Service Company, 211 E. 7th Street, Suite 620, Austin, TX 78701-3218.

3. On information and belief, NXP Semiconductors N.V. is a corporation organized

under the laws of the Netherlands, having its principal place of business at High Tech Campus 60, 5656 AG Eindhoven, the Netherlands.

4. On information and belief, NXP B.V. is a corporation organized under the laws of the Netherlands, having its principal place of business at High Tech Campus 60, 5656 AG Eindhoven, the Netherlands.

5. On information and belief, NXP B.V. is a direct wholly owned subsidiary of NXP Semiconductors N.V. and NXP USA, Inc. operates as a subsidiary of NXP B.V. and are a part of the same corporate structure and distribution chain for the making, selling, offering to sell, selling, and using of infringing devices in the United States, including in the State of Texas and this judicial district.

6. On information and belief, Defendants further share the same ownership, management, advertising platforms, facilities, distribution chains and platforms, infringing product lines, and products involving relevant technologies.

7. On information and belief, Defendants operate as a unitary business and are jointly and severally liable for the acts of patent infringement alleged herein.

JURISDICTION AND VENUE

8. This is an action under the patent laws of the United States, 35 U.S.C. §§ 1, et seq., for infringement by NXP of claims of U.S. Patent Nos. 6,480,021, 6,820,234, 7,107,386, 7,278,069, and 7,426,603 ("the Patents-in-Suit").

9. This Court has subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a).

10. NXP is subject to personal jurisdiction of this Court because, inter alia, on information and belief, independently and/or via its agents, (i) NXP sells and offers for sale its

products in Texas, (ii) NXP sells and offers for sale its products by using distributors and sales representatives located in Texas; and/or (iii) NXP places its products in the stream of commerce with intent or knowledge that those products would end up in Texas. In addition, or in the alternative, this Court has personal jurisdiction over NXP Semiconductors N.V. and NXP B.V. pursuant to Fed. R. Civ. P. 4(k)(2).

11. Venue is proper as to NXP Semiconductors N.V. and NXP B.V. in this district under 28 U.S.C. § 1391(c) because, inter alia, NXP Semiconductors N.V. and NXP B.V. are foreign corporations.

12. Venue is proper in this district as to NXP USA, Inc. under 28 U.S.C. § 1400(b) because (i) NXP USA, Inc. has committed and continues to commit acts of patent infringement by, inter alia, offering for sale and selling, on their own and as part of a device, infringing NXP USA, Inc. products; and (ii) has regular and established places of business in this district, including at 3501 Ed Bluestein Boulevard, Austin, TX 78721, 6501 West William Cannon Drive, Austin, TX 78735, and 810 Hesters Crossing Road, Round Rock, TX 78681.

BACKGROUND

13. On November 12, 2002, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 6,480,021 ("the '021 Patent"), entitled "Transmitter Circuit Comprising Timing Deskewing Means."

14. Alexander Roger Deas, Vasily Grigorievich Atyunin, and Igor Anatolievich Abrossimov, invented the technology claimed in the '021 Patent.

15. On November 16, 2004, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 6,820,234 ("the '234 Patent"), entitled "Skew Calibration Means And A Method Of Skew Calibration."

16. Alexander Roger Deas, Ilya Valerievich Klotchkov, Igor Anatolievich Abrossimov, and Vasily Grigorievich Atyunin invented the technology claimed in the '234 Patent.

17. On September 12, 2006, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 7,107,386 ("the '386 Patent"), entitled "Memory Bus Arbitration Using Memory Bank Readiness."

18. Stephen Clark Purcell and Scott Kimura invented the technology claimed in the '386 Patent.

19. On October 2, 2007, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 7,278,069 ("the '069 Patent"), entitled "Data Transmission Apparatus For High-Speed Transmission Of Digital Data and Method For Automatic Skew Calibration."

20. Igor Anatolievich Abrosimov, Vasily Grigorievich Atyunin, Alexander Roger Deas, and Ilya Vasilievich Klotchkov invented the technology claimed in the '069 Patent.

21. On September 16, 2008, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 7,426,603 ("the '603 Patent"), entitled "Memory Bus Arbitration Using Memory Bank Readiness."

22. Stephen Clark Purcell and Scott Kimura invented the technology of the '603 Patent.

23. CCO is the assignee and owner of the right, title, and interest in and to the Patents-in-Suit, including the right to assert all causes of action arising under said patents and the right to any remedies for infringement.

NOTICE

24. By letter dated June 10, 2019, CCO notified NXP of the existence of the Patents-in-Suit, and of infringement of the '234; '386; '069; and '603 Patents by NXP. CCO's letter identified exemplary infringing NXP products and an exemplary infringed claim for each of the '234; '386; '069; and '602 Patents. CCO's June 10, 2019 letter invited NXP to hold a licensing discussion with CCO.

25. By email dated July 8, 2019, NXP acknowledged receipt of CCO's June 10, 2019 letter and requested claim charts identifying infringement by NXP.

26. By letter dated May 1, 2020, CCO provided seven claim charts to NXP, illustrating infringement by various NXP products of each of the Patents-in-Suit.

27. By email dated June 12, 2020, NXP responded that it had reviewed CCO's claim charts but stated that it does not see justification for taking a license to CCO's patents.

LICENSING

28. As of the time of this Complaint, CCO has entered into licensing agreements relating to the Patents-in-Suit with at least Arastu Systems, NVIDIA, Qualcomm, Via Technologies, Rockchip, and Socionext.

COUNT I: INFRINGEMENT OF THE '021 PATENT

29. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

30. On information and belief, NXP has infringed the '021 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States, or importing into the United States certain processors, microcontrollers, and Systems-on-Chip that include DDR3, DDR4, LPDDR3, and LPDDR4 memory controller systems ("DDR Controller") (collectively, "Accused NXP Products").

31. On information and belief, NXP has infringed at least claim 11 of the '021 Patent by performing a method of eliminating skew caused by inter-symbol interference and cross-talk influence in the transmission line for high-speed transmission of digital data by modifying delays at each DQ line of an exemplary DDR Controller, such as an LPDDR4 Controller incorporated in the Accused NXP Products, including during regular operation and during development, design, testing, and verification of the Accused NXP Products, in part because they operate in compliance with LPDDR4 JEDEC standard. Ex. 1 at 7 (NXP Semiconductors, i.MX 8QuadPlus Automotive and Infotainment Applications Processors, Data Sheet: Technical Data); Ex. 2 at 6 (NXP Semiconductors, Mask Set Errata for Mask 1N94W, Oct. 2019); Ex. 8 at 195 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017); Ex. 14 (www.intel.cn website).

32. On information and belief, the NXP DDR Controller continuously transmits data through each transmission line, such as DQ transmission line, provided by at least one driver. Ex. 2 at 6 (NXP Semiconductors, Mask Set Errata for Mask 1N94W, Oct. 2019); Ex. 1 at 7 (NXP Semiconductors, i.MX 8QuadPlus Automotive and Infotainment Applications Processors, Data Sheet: Technical Data, Oct. 2019); Ex. 8 at 195 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017).

33. On information and belief, the NXP DDR Controller measures a skew for the transmitted DQ bit patterns by training write boundaries of a data eye during write leveling. Ex. 8 at 195 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017) ("After writing data to the SDRAM with the MPC [Write DQ FIFO] command, the data can be read back with the MPC [Read DQ FIFO] command and results compared with "expect" data to see if further training (DQ Delay) is needed.").

34. On information and belief, the NXP DDR Controller records and stores

information on skew caused by inter-symbol interference and cross-talk influence in the DQ transmission lines for at least one data pattern transmitted through the transmission line. *Id.*; Ex. 14 (intel.cn website).

35. On information and belief, the NXP DDR Controller generates and applies a correction to the timing position of a signal transition between two logical levels, the correction being generated on the basis of the information stored in the storage means, so as to compensate for the above skew. Ex. 8 at 195 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017).

36. On information and belief, NXP has induced, and continues to induce, infringement of the '021 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, infringing NXP products that incorporate the DDR Controller. NXP had the knowledge of the '021 Patent, at least from the time of receiving CCO's May 1, 2020 notice of infringement, and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the Accused NXP Products, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

37. On information and belief, NXP has committed the foregoing infringing activities without a license.

38. On information and belief, NXP's infringing activities commenced within six years prior to the filing of this complaint, entitling CCO to past damages.

39. On information and belief, NXP knew the '021 Patent existed, knew of its claims,

and knew of NXP's infringing products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '021 Patent.

COUNT II: INFRINGEMENT OF THE '234 PATENT

40. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

41. On information and belief, NXP has infringed the '234 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States, or importing into the United States the Accused NXP Products.

42. For example, on information and belief, NXP has infringed at least claim 28 of the '234 Patent by making, using, offering to sell, selling in the United States, or importing into the United States the Accused NXP Products that include the DDR Controller, such as DDR3, DDR4, LPDDR3, and LPDDR4 Memory Controller Systems, with a timing uncertainty reduction system for calibration of a high speed communication apparatus, including during development, design, testing, and verification of the Accused NXP Products and specifically the DDR Controller. Ex. 4 at 63, 65 (NXP Semiconductors, QorIQ LS1024A Data Sheet, Jan. 2018); Ex. 1 at 7-8, 51 (NXP Semiconductors, i.MX 8QuadPlus Automotive and Infotainment Applications Processors, Data Sheet: Technical Data, Oct. 2019); Ex. 2 at 1 (NXP Semiconductors, Mask Set Errata for Mask 1N94W, Oct. 2019).

43. On information and belief, an exemplary DDR Controller reduces timing uncertainty in DDR3, DDR3L, DDR4 and LPDDR4 memory transmission including calibration using the Multi-Purpose Register (MPR), read centering, write centering, and write leveling. Ex. 5 at 48 (NXP, Fundamentals of DDR in QorIQ Processing Platforms, Apr. 2014); Ex. 10 at 8, 37 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012); Ex. 9 at 17, 48-51 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008); Ex. 11 at 55 (DDR PHY Interface, DFI 4.0

Specification); Ex. 8 at 26, 190, 195 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017); Ex. 7 at 68, 61 (JEDEC Standard, LPDDR3, JESD209-3C, Aug. 2015).

44. On information and belief, the DDR Controller comprises at least one driving register for latching transmitted DQ signals, with a plurality of inputs and outputs. Ex. 3 at 65 (NXP Semiconductors, QorIQ LS1024A Data Sheet, Jan. 2018); Ex. 12 at 67 (C. Kim et al., High-Bandwidth Memory Interface); Ex. 1 at 7 (NXP Semiconductors, i.MX 8QuadPlus Automotive and Infotainment Applications Processors, Data Sheet: Technical Data, Oct. 2019).

45. On information and belief, the DDR Controller further comprises at least one receiving register for latching received DQ signals, with a plurality of inputs and outputs. Ex. 3 at 65 (NXP Semiconductors, QorIQ LS1024A Data Sheet, Jan. 2018); Ex. 12 at 67 (C. Kim et al., High-Bandwidth Memory Interface); Ex. 13 at 13 (Technical Note, High-Speed DRAM Controller Design, Micron); Ex. 1 at 7 (NXP Semiconductors, i.MX 8QuadPlus Automotive and Infotainment Applications Processors, Data Sheet: Technical Data, Oct. 2019).

46. On information and belief, the DDR Controller includes a main clock (such as the MC Clock) for generating a main clock signal. Ex. 1 at 30 (NXP Semiconductors, i.MX 8QuadPlus Automotive and Infotainment Applications Processors, Data Sheet: Technical Data, Oct. 2019); Ex. 11 at 120 (DDR PHY Interface, DFI 4.0 Specification).

47. On information and belief, the DDR Controller includes a reference clock, such as an internal clock or a PHY clock, for generating a reference signal for calibrating the receiving register or registers, such as during DQ read centering/read training; said reference clock being associated with the main clock signal. Ex. 11 at 120, 146-147 (DDR PHY Interface, DFI 4.0 Specification); Ex. 13 at 12 (Technical Note, High-Speed DRAM Controller Design, Micron); Ex. 3 at 73 (NXP Semiconductors, QorIQ LS1024A Data Sheet, Jan. 2018); Ex. 5 at 48 (NXP,

Fundamentals of DDR in QorIQ Processing Platforms, Apr. 2014); Ex. 16 at 1 (NXP Semiconductors, Mask Set Errata for Mask 0N14W, May 2018); Ex. 1 at 30 (NXP Semiconductors, i.MX 8QuadPlus Automotive and Infotainment Applications Processors, Data Sheet: Technical Data, Oct. 2019); Ex. 2 at 6-8 (NXP Semiconductors, Mask Set Errata for Mask 1N94W, Oct. 2019); Ex. 8 at 190, 195 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017); Ex. 7 at 61 (JEDEC Standard, LPDDR3, JESD209-3C, Aug. 2015).

48. On information and belief, the DDR Controller includes phase shift circuitry to align the timing of the driving signals' relative to the CK signal at the destination, such as phase shift circuitry aligning the timing of the DQS signals via write leveling, or DQ signals following write centering. Ex. 6 at 25 (NXP Freescale Technology Forum, DDR Basics, Register Configurations & Pitfalls, Jul. 2009); Ex. 10 at 31-33 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012); Ex. 9 at 42-43 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008); Ex. 11 at 157 (DDR PHY Interface, DFI 4.0 Specification); Ex. 2 at 6 (NXP Semiconductors, Mask Set Errata for Mask 1N94W, Oct. 2019); Ex. 8 at 186 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017); Ex. 7 at 68 (JEDEC Standard, LPDDR3, JESD209-3C, Aug. 2015).

49. On information and belief, NXP has induced, and continues to induce, infringement of the '234 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, infringing NXP products that incorporate the DDR Controller. NXP had the knowledge of the '234 Patent, at least from the time of receiving CCO's June 10, 2019, notice of infringement, and acted with specific intent to encourage its customers and end users to make,

use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the DDR Controller, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

50. On information and belief, NXP has committed the foregoing infringing activities without a license.

51. On information and belief, NXP's infringing activities commenced within six years prior to the filing of this complaint, entitling CCO to past damages.

52. On information and belief, NXP knew the '234 Patent existed, knew of its claims, and knew of NXP's infringing products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '234 Patent.

COUNT III: INFRINGEMENT OF THE '386 PATENT

53. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

54. On information and belief, NXP has infringed the '386 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States the Accused NXP Products.

55. For example, on information and belief, NXP has infringed at least claim 1 of the '386 Patent by making, using, offering to sell, selling in the United States or importing into the United States infringing NXP Products, which include the DDR Controllers, such as DDR3, DDR4, LPDDR3, and LPDDR4 Memory Controller Systems, adapted to send a plurality of memory transactions over a memory bus to a memory having a plurality of memory banks. Ex. 4 at 3830-1, 3835, 3838, 3870, 3879, (i.MX 6Dual/6Quad Applications Processor Reference Manual, Jun. 2014); Ex. 9 at 15-16 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008);

Ex. 19 at 1 (i.MX 8M Dual / 8M QuadLite / 8M Quad Applications Processors Data Sheet for Consumer Products, Data Sheet: Technical Data, NXP Semiconductors, May, 2018); Ex. 20 at 3 (Micron Memory Support for NXP i.MX 8M Platforms, NXP, Micron, 2019); Ex. 10 at 7 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012); Ex. 7 at 16 (JEDEC Standard, LPDDR3, JESD209-3C, Aug. 2015); Ex. 8 at 19 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017).

56. On information and belief, the DDR Controller comprises a queue comprising a plurality of request stations, wherein each of the plurality of memory transactions is stored in one of the request stations and is addressed to one of the plurality of memory banks. Ex. 4 at 3830, 3837-8 (i.MX 6Dual/6Quad Applications Processor Reference Manual, Jun. 2014); Ex. 9 at 33 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008); Ex. 10 at 24 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012); Ex. 7 at 80 (JEDEC Standard, LPDDR3, JESD209-3C, Aug. 2015); Ex. 8 at 246 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017).

57. On information and belief, the DDR Controller includes an arbiter, such as the memory controller IP block, coupled to each of the plurality of request stations, adapted to select any of the plurality of memory transactions. Ex. 4 at 3830-1 (i.MX 6Dual/6Quad Applications Processor Reference Manual, Jun. 2014).

58. On information and belief, the arbiter of the DDR Controller is configured to generate a plurality of bank readiness signals, each bank readiness signal indicating the readiness of one of the plurality of memory banks to accept a memory transaction, and, based on the bank readiness signals, is configured to select one of the memory transactions for transmission over the memory bus. Ex. 4 at 3835 (i.MX 6Dual/6Quad Applications Processor Reference Manual, Jun. 2014); Ex. 9 at 18, 55 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008); Ex. 10

at 9, 82 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012); Ex. 7 at 16, 35 (JEDEC Standard, LPDDR3, JESD209-3C, Aug. 2015); Ex. 8 at 18, 58 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017).

59. On information and belief, NXP has induced, and continues to induce, infringement of the '386 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States the DDR Controller. NXP had the knowledge of the '386 Patent, at least from the time of receiving CCO's June 10, 2019, notice of infringement, and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the DDR Controller, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

60. On information and belief, NXP has committed the foregoing infringing activities without a license.

61. On information and belief, NXP's infringing activities commenced within six years prior to the filing of this complaint, entitling CCO to past damages.

62. On information and belief, NXP knew the '386 Patent existed, knew of its claims, and knew of NXP infringing products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '386 Patent.

COUNT IV: INFRINGEMENT OF THE '069 PATENT

63. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

64. On information and belief, NXP has infringed the '069 Patent pursuant to 35

U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States, or importing into the United States the Accused NXP Products.

65. For example, on information and belief, NXP has infringed at least claim 12 of the '069 Patent by performing a method for automatic skew calibration of a transmission apparatus for high speed transmission of digital data, comprising a transmitter and a receiver, including during development, design, testing, and verification of the Accused NXP Products, which include the DDR Controllers, such as a DDR3, DDR4, LPDDR3, and LPDDR4 memory controllers that automatically calibrate skew. Ex. 3 at 65 (NXP Semiconductors, QorIQ LS1024A Data Sheet, Jan. 2018); Ex. 12 at 67 (C. Kim et al., High-Bandwidth Memory Interface); Ex. 6 at 25 (NXP Freescale Technology Forum, DDR Basics, Register Configurations & Pitfalls, Jul. 2009); Ex. 10 at 8, 31 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012); Ex. 9 at 17, 27 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008); Ex. 11 at 157 (DDR PHY Interface, DFI 4.0 Specification); Ex. 1 at 7 (NXP Semiconductors, i.MX 8QuadPlus Automotive and Infotainment Applications Processors, Data Sheet: Technical Data, Oct. 2019); Ex. 2 at 6 (NXP Semiconductors, Mask Set Errata for Mask 1N94W, Oct. 2019); Ex. 8 at 26 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017); Ex. 7 at 68 (JEDEC Standard, LPDDR3, JESD209-3C, Aug. 2015).

66. The DDR Controller calibrates registers of the receiver in relation to a reference clock edge. Ex. 3 at 48, 65, 73 (NXP Semiconductors, QorIQ LS1024A Data Sheet, Jan. 2018); Ex. 13 at 12 (Technical Note, High-Speed DRAM Controller Design, Micron); Ex. 11 at 120, 144, 146-7 (DDR PHY Interface, DFI 4.0 Specification); Ex. 1 at 7, 30 (NXP Semiconductors, i.MX 8QuadPlus Automotive and Infotainment Applications Processors, Data Sheet: Technical Data, Oct. 2019); Ex. 2 at 1 (NXP Semiconductors, Mask Set Errata for Mask 1N94W, Oct.

2019).

67. The DDR Controller calibrates propagation delays of registers of the transmitter, using the calibrated registers of the receiver, such as the registers calibrated to receive the samples of CK_t – CK_c during write leveling. Ex. 6 at 25 (NXP Freescale Technology Forum, DDR Basics, Register Configurations & Pitfalls, Jul. 2009); Ex. 10 at 31 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012); Ex. 9 at 42 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008); Ex. 11 at 157 (DDR PHY Interface, DFI 4.0 Specification); Ex. 1 at 7 (NXP Semiconductors, i.MX 8QuadPlus Automotive and Infotainment Applications Processors, Data Sheet: Technical Data, Oct. 2019); Ex. 15 (community.nxp.com website); Ex. 8 at 186 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017); Ex. 7 at 68 (JEDEC Standard, LPDDR3, JESD209-3C, Aug. 2015).

68. On information and belief, the DDR Controller's calibration is performed by measuring time offsets between different signals that form a communication channel. Ex. 6 at 25 (NXP Freescale Technology Forum, DDR Basics, Register Configurations & Pitfalls, Jul. 2009); Ex. 10 at 30-31, 33 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012); Ex. 9 at 40, 42-43 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008); Ex. 11 at 144-5 (DDR PHY Interface, DFI 4.0 Specification); Ex. 8 at 186, 244 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017); Ex. 1 at 51 (NXP Semiconductors, i.MX 8QuadPlus Automotive and Infotainment Applications Processors, Data Sheet: Technical Data, Oct. 2019); Ex. 7 at 68 (JEDEC Standard, LPDDR3, JESD209-3C, Aug. 2015).

69. On information and belief, the DDR Controller applies the measured time offsets to compensate for the inter-signal skew by performing relative alignment of the measured offsets to a main clock edge. Ex. 6 at 25 (NXP Freescale Technology Forum, DDR Basics, Register

Configurations & Pitfalls, Jul. 2009); Ex. 10 at 32-33 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012); Ex. 9 at 42-43 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008); Ex. 8 at 186 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017); Ex. 7 at 68 (JEDEC Standard, LPDDR3, JESD209-3C, Aug. 2015); Ex. 11 at 157 (DDR PHY Interface, DFI 4.0 Specification).

70. On information and belief, NXP has induced, and continues to induce, infringement of the ’069 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, infringing NXP products that incorporate the DDR Controller. NXP had the knowledge of the ’069 Patent, at least from the time of receiving CCO’s June 10, 2019, notice of infringement, and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the DDR Controller, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

71. On information and belief, NXP has committed the foregoing infringing activities without a license.

72. On information and belief, NXP’s infringing activities commenced within six years prior to the filing of this complaint, entitling CCO to past damages.

73. On information and belief, NXP knew the ’069 Patent existed, knew of its claims, and knew of NXP infringing products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the ’069 Patent.

COUNT V: INFRINGEMENT OF THE '603 PATENT

74. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

75. On information and belief, NXP has infringed the '603 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States the Accused NXP Products.

76. For example, on information and belief, NXP has infringed at least claim 16 of the '603 Patent by performing a method of using a multiplexer to manage the transmission of a plurality of memory transactions to a memory having a plurality of memory banks, including during development, design, testing, and verification of the Accused NXP Products, which include the DDR Controller, such as a DDR3, DDR4, LPDDR2, and LPDDR4. Ex. 19 at 1 (i.MX 8M Dual / 8M QuadLite / 8M Quad Applications Processors Data Sheet for Consumer Products, Data Sheet: Technical Data, NXP Semiconductors, May, 2018); Ex. 20 at 3 (Micron Memory Support for NXP i.MX 8M Platforms, NXP, Micron, 2019); Ex. 4 at 352, 3831 (i.MX 6Dual/6Quad Applications Processor Reference Manual, Jun. 2014); Ex. 9 at 15 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008); Ex. 10 at 7 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012); Ex. 7 at 16 (JEDEC Standard, LPDDR3, JESD209-3C, Aug. 2015); Ex. 8 at 19 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017).

77. On information and belief, the multiplexer used by the NXP DDR Controller comprises a plurality of multiplexer inputs for receiving the plurality of memory transactions and a multiplexer output for sending each of the plurality of memory transactions to the memory. *See id*.

78. On information and belief, the NXP DDR Controller receives a plurality of memory transactions at the multiplexer inputs, wherein each memory transaction is addressed to

a corresponding memory bank, in accordance with the respective JEDEC standards for each DDR Controller. Ex. 4 at 3835, 3838 (i.MX 6Dual/6Quad Applications Processor Reference Manual, Jun. 2014); Ex. 9 at 33 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008); Ex. 10 at 24 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012); Ex. 7 at 80 (JEDEC Standard, LPDDR3, JESD209-3C, Aug. 2015); Ex. 8 at 246 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017).

79. On information and belief, the NXP DDR Controller associates a priority with each received memory transaction. Ex. 4 at 3831 (i.MX 6Dual/6Quad Applications Processor Reference Manual, Jun. 2014).

80. On information and belief, the NXP DDR Controller generates a plurality of bank readiness signals indicating the readiness of each memory bank available to accept a memory transaction, wherein the plurality of bank readiness signals are based on the plurality of memory transactions at the multiplexer inputs and the multiplexer output, in accordance with the respective JEDEC standards for each DDR Controller. Ex. 4 at 3835 (i.MX 6Dual/6Quad Applications Processor Reference Manual, Jun. 2014); Ex. 9 at 18, 55 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008); Ex. 10 at 9, 82 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012); Ex. 7 at 16, 35 (JEDEC Standard, LPDDR3, JESD209-3C, Aug. 2015); Ex. 8 at 18, 58 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017).

81. On information and belief, the NXP DDR Controller sends each of the plurality of memory transactions to its corresponding memory banks via the multiplexer output based on the associated priorities and the bank readiness signals. Ex. 4 at 352, 3835, 3869 (i.MX 6Dual/6Quad Applications Processor Reference Manual, Jun. 2014).

82. On information and belief, the NXP DDR Controller prioritizes each memory

transaction based on the memory transaction's position in a queue. Ex. 4 at 3831 (i.MX 6Dual/6Quad Applications Processor Reference Manual, Jun. 2014).

83. On information and belief, NXP has induced, and continues to induce, infringement of the '603 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States the DDR Controller. NXP had the knowledge of the '603 Patent, at least from the time of receiving CCO's June 10, 2019, notice of infringement, and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the DDR Controller, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

84. On information and belief, NXP has committed the foregoing infringing activities without a license.

85. On information and belief, NXP's infringing activities commenced within six years prior to the filing of this complaint, entitling CCO to past damages.

86. On information and belief, NXP knew the '603 Patent existed, knew of its claims, and knew of NXP's infringing products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '603 Patent.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff CCO prays for the judgment in its favor against NXP, and specifically, for the following relief:

A. Entry of judgment in favor of CCO against NXP on all counts;

B. Entry of judgment that NXP has infringed the Patents-in-Suit;

C. Entry of judgment that NXP's infringement of the Patents-in-Suit has been willful;

D. An order permanently enjoining NXP from infringing the Patents-in-Suit;

E. Award of compensatory damages adequate to compensate CCO for NXP's infringement of the Patent-in-Suit, in no event less than a reasonable royalty trebled as provided by 35 U.S.C. § 284;

F. Award of CCO's costs;

G. Pre-judgment and post-judgment interest on CCO's award; and

H. All such other and further relief as the Court deems just or equitable.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38 of the Fed. R. Civ. P., Plaintiff CCO hereby demands trial by jury in this action of all claims so triable.

Respectfully Submitted,

February 9, 2021

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